IWFIPT 2001

European Commission -
US National Science Foundation

Strategic Research Workshop

International Workshop

Future Information Processing Technologies

Gubbio, Italy, 3-6 September 2001

Workshop Report

International Workshop on Future Information Processing Technologies (IWFIPT-2001) Gubbio, Italy, September 3-6, 2001

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1. Preface

The semiconductor market has grown at an annual average rate of approximately 15% over the past three and a half decades, driven primarily by an exponential decrease in cost per function and an improved performance, mainly resulting from device miniaturization. Despite the present downturn in the world economy, such a phe-nomenal trend is expected to continue in the next decade and beyond, as predicted by the International Technology Roadmap for Semicon-ductors (ITRS). A key milestone of this evolution is going to be the 100 nm minimum-feature-size node, which is going to be reached in year 2004. Moreover, the obstacles down to the 35 nm range are likely to be overcome in the near future, notwithstanding formidable scientific, technical, organizational and financial problems to be solved. At that point chips will contain 2 billion logic transistors, or the equivalent of 2.000 programmable processors embedded in a re-configurable network and a large amount of memory. Thus, the real bottleneck is probably going to be our ability to design products and services exploiting such huge multiprocessor architectures on a single piece of silicon.

Progress in sub-100 nm technology, DSP, MEMS and RF CMOS is expected to cause a paradigm shift in the ICT world referred to as the post-PC era, when wearable computing augments our consciousness, protects our health and globally connects people and things. To date, the driving force of electronics is global broad-band networking at all levels, from the optical fiber backbone to the wired and wireless last kilometer, down to the body area network that connects the individual to an adaptive intelligent environment. Designing such systems differs radically from designing CPU architectures. The art will be to design a diversity of cheap, energy efficient, yet programmable platforms that can be configured over the Internet and communicate with humans through non-keyboard interfaces. This will require a grand convergence of previously separated domains of expertise, such as programmable-reconfigurable multi-processor architectures with embedded software, broadband radio, MEMS and biosensor interfaces.

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2. Aims and format

The aim of the International Workshop on Future Information Processing Technologies (IWFIPT) is that of bringing together top-level scientists and strategic thinkers from all around the world, to debate research and technology frontiers that hold promise to extend progress in information processing into the 21st century. The format has been chosen to be that of a Gordon-type conference, in order to promote openness in discussions and a completely free exchange of ideas. Participation is typically limited to 30 European, 30 American and 30 Asian people. All sessions have a main subject and are driven by invited presentations delivered by leading scientists from Europe, USA and Far East and are followed by a collective discussion and a wrap-up led by the session chairman. All invited participants, with exclusion of keynote speakers, are requested to exhibit a poster. The chosen location is expected to favor informal and fruitful interaction among participants.

The International Scientific Committee of IWFIPT comprises leading European, American and Asian scientists from Industry and Academia, and the organization of the workshop is centrally and jointly coordinated by the by the European Commission, the NSF, the Semiconductor Re-search Corporation (SRC) from USA and by the Semiconductor Industry Research Institute (SIRIJ) and the Semiconductor Technology Academic Research Center (STARC) from Japan.

For those interested in the details of the 4th IWFIPT, including the workshop program, the presentation materials, and a meeting summary, this information is available on the web site www.iwfipt.unibo.it.

3. Selected topics

Previous workshops emphasized the technical challenges that must be faced in order to develop the enabling technology which is needed to proceed along the Technology Roadmap. Among these, the limits of optical lithography and its possible replacements, on-chip power dissipation, signal delay due to interconnects and the non-scalability of the oxide thickness did appear as some of the most important hurdles to be overcome.

New opportunities resulting from nanotechnology, quantum devices, molecular arrays and biological systems were also addressed as emerging and promising areas. In addition, an increasing need for an early system approach which demands for inter-disciplinary efforts was defined, to allow for the early assessment of the opportunities of new concepts and methodologies. In this workshop, more attention is devoted to system aspects and a key to new applications is expected to be the human interface and the trend towards person-centric, portable systems.

The selected topics in the 4^{th} IWFIPT are: “Future system and technology challenges” (two sessions) where emphasis is placed on the convergence among PCs, PDA, cell phones and the related network infrastructure; “Silicon evolution”, which addresses system on chip design challenges, reconfigurable computing and low-power design issues; “Enabling technologies”, such as optical networking and the human interface and, finally, “Emerging technologies”, addressing new systems and technology concepts including smart dust, super-conducting devices and new implementations of quantum computers.

4. Future systems and technology challenges I

This session comprised three invited presentations. The first one: “The ultimate personal companion”, was given by Heikki Huomo from Nokia Research, Finland, and addressed the current evolution of the cellular/mobile communication towards its 3rd generation. This evolution is taking place together with wireless access to corporate and other private LAN’s, as standards and interoperability issues are getting resolved. The next frontier of open system development seems to be in the area of peer-to-peer networking between devices around the personal terminal carried by people. As the PAN paradigm matures, it will transform the voice communication oriented terminal to become the ultimate personal companion. This presentation specifically focused on the challenges and open research items in this very area.

The second keynote presentation entitled: “Ubiquitous networking, wireless beyond 3G” was given by Jan Kruys from Agere Systems, USA, and dealt with the expected changes in computing and network that will shape the evolution of wireless communications: semantic web, ubiquitous computing and human need for personal communications. Today, the web is basically a repository of data, expressed in all types of format, mostly HTML. The semantic web will hold data plus knowledge about the data, which allows for active searching using script. This will lead to changing communication patterns from a download-oriented to a transaction-oriented scheme. Voice service will never decline and is expected to be a major growth area. Video will remain a secondary revenue source as the videophone limits the user’s freedom, although in amusement and private settings other factors may dominate. The implications are: i) Networking will be-come decoupled from location and from devices like PCs; ii) Voice and voice plus data (conferencing) will be the primary revenue source for the mobile operators and, iii) Data-base services will far outpace voice and rt-video based services in the professional world. The killer applications of the future will be service ubiquity, robustness and quality of service (QoS).

The evolution of the network will occur along the following lines: GSM will expand into data space with GPRS, but sending packets over a circuit-switched system is not very efficient; UMTS is supposedly multimedia, but its underlying structure remains circuits switching and is not efficient for services using the IP protocol; claims of high data rates are dwarfed by wireless LANs, but it will become the mainstream of mobile systems. The wireless LAN will be dominated by the IEEE 802.11 standard, which is robust against interference, and designed for access to a shared medium with full connectivity. It started at 2 Mb/sec in the early 1990’s and is now getting ready for 54 Mb/sec.

Wireless communications will change to a tiered structure that sup-ports both high speed, but short range, communications and long range communications at much

lower data rates. The user will be spared much of the details of dealing with different networks accessible with multi-mode terminals made possible by advances in technology. These include advanced, low power ASICs, MIMO transmission systems and IPv6.

The third invited presentation in this session was entitled: “Digital home networks” and was given by Ryoichi Sugimura from Panasonic OWL, Japan. Based on a few assumptions on the hardware network infrastructure in the home of the future, this presentation addressed possible promising applications within the domestic environment, from the ability to detect the home approach of the owner from his GPS supporting mobile phone, to the performance of a number of services, such as turning on the lighting and heating systems, opening the garage, cooking and delivering the preferred music or playing performance, all the way down to activating the security mode before getting asleep. The presentation also examined possible end-to-end architectures required to support these new applications.

5. Future systems and technology challenges II

This session comprised three invited presentations. The first one: “Optical network Internet infrastructure”, was given by Toshitaka Tsuda, from Fujitsu, Japan and addressed the current status of the optical network and its likely evolution in the future. In order to support the explosive increase of the Internet traffic, the optical network will evolve along three main directions, namely: more capacity, longer distance, and all-optical networking. Currently, transistor speed is not fast enough, fiber characteristics and noise accumulation should be compensated, and optical switching is still difficult. Based on the above scenario, technology is evolving toward a combination of high-speed transmission rates (above 10 Gb/sec) and dense Wave-length Division Multiplex (WDM) technology which can provide the rate of capacity increase which is needed to sustain the demand. This evolution, however, will require the development of new photonic devices.

The second keynote presentation in this session was entitled: “Technology challenges for the 2020 car” and was given by Gerhard Hettich, from Daimler Chrysler, Germany. After nearly 100 years of continuous vehicle development, at the mid of the eighties the electronic revolution came along. In the next ten years all key functions in vehicles were progressively controlled by electronic devices. In addition, the number of functions was increased to some hundreds, including resource protection, increased safety and comfort and all kind of infotainment. To date, the added value of electronics is becoming the most important part for a vehicle manufacturer.

Based on this, the automotive researchers are now focused on tasks which are closer to computer science, information technology and semiconductor research than to the well known vehicle technology. There is, however, a main difference compared to other research fields. The car users are not car experts and they trust the manufacturer’s capability to keep them safe and comfortable under all conditions. They expect that all car systems work properly and all functions be available at a reasonable price. All future systems have to comply with this expectation; this means that functionality and dependability must be looked upon very closely.

This leads to two growing research fields for the coming years: i) In-car technology as electric/electronic architecture, mechatronic and telematics and, ii) Car-to-environment based technologies, like emission control, resource protection, accident-reduced driving and traffic management. According to the author, technology challenges are going to be design methods and tools for distributed-safety systems; failure correction for distributed systems in hardware and software with 100% reliability of the vehicle function; high speed failure correcting systems with different physical layers for internal and external communication; autonomous acting subsystems with intelligent abilities connected to internal and external car

systems; plug and play systems with self-configuration abilities in hardware and software; new smart actuators with less weight and higher efficiency; driver assistant systems for safety and human-machine interface. The focus on safety and reliability is such that the world of electronics as a whole may possibly learn from the automotive research field.

The third keynote presentation, entitled: “At the interface between technology and biology”, was given by Robert Austin, Princeton University, USA. This presentation showed the growing potential of nanoelectronics in biological studies, with a specific application to the mapping of gene expression. The new nanotechnologies allow in fact for single cell mapping of the epigenetic state of a cell, i.e. the combination of genome and protein control factors which together determine the biological state of a cell. According to the author, the real challenge in these studies is to characterize critical control gene states at the single cell level, not some sort of a global average as is presently being done by many scientists. This goal is being pursued in the illustrated example by back illumination of a slit nanofabricated in an aluminum film and by excitation of fluorescent tags as a stretched DNA molecule passes transverse to the slit in the evanescent field.

An interdisciplinary spirit will guide those excited by the global analysis of protein function. Geneticists need to talk to chemists, physiologists to physicists, cell biologists to computer scientists. With questions so grand, the expertise to answer them requires the entire spectrum of science. This combination of new technologies and its widespread dispersion together with broad-ranging collaborative projects will culminate when the undertaking that began with genome sequencing reaches fruition.

Although the human genome has been sequenced, at some level, it is misleading to think that we now understand how the genome is expressed and how the cell functions. This is an incredibly complex system, which requires a massive amount of knowledge to master. The author’s goal is to contribute to the tool development which will help biologists attack the fundamental heterogeneity and uniqueness of each cell.

According to the author, the future could possibly lead us to: i) Annotate the massive amount of information about the epigenetic state of single cells as a function of time and body state; ii) Predict the complex interactions between protein networks in the cell by detailed network modeling; iii) Allow us to do genetic intervention, i.e. insertion of genetically modified material into the genome to correct “mistakes” and, iv) Put an end to aging at some stage in development.

6. Silicon Evolution

The first keynote presentation in this session entitled “Low Power CMOS Design” was delivered by Tadahiro Kuroda, Keio University, Japan, and was focused on the problem of power dissipation in silicon chips. This problem is due to the growing integration level and system complexity made possible by the current and future silicon technologies. The increased power dissipation per unit area requires an efficient heat extraction from small-area devices; hence, expensive packages. Besides, for portable and wearable functional units, a low-power dissipation as a whole is needed to ensure a long battery functionality.

Since there is no new energy efficient device on the horizon other than the MOSFET, low power CMOS design is essential until a new technology becomes available. The principles for power reduction stem from a simple and well-known expression for power dissipation in CMOS circuits. The main strategies are: i) Lowering the switching probability of a circuit by gated clocks, optimized CAD design and low-transition coding; ii) Lowering the load capacitance by technology scaling, gate sizing, low-_ dielectrics and embedded memory; iii) Lowering the supply voltage by variable V_{DD} and V_{TH}, low-voltage memory design and low-swing clock busses and, iv) Lowering the operating frequency by using better algorithms. The presentation thus addressed the perspective of a future low-power CMOS design from the standpoints of both system requirements and design issues.

The second presentation entitled: “System-on-chip design challenges for the post PC era” was delivered by Hugo De Man, from IMEC, Belgium. According to the author, the driving force of electronics is now global broad-band networking at all levels, from the optical fiber backbone to the wired and wireless last kilometer down to the body area network that connects the individual to an adaptive intelligent environment. Designing such systems differs radically from designing CPU architectures. The art will be to design a diversity of cheap, energy efficient, yet programmable platforms that can be configured over the Internet and communicate with humans through non-keyboard interfaces. This requires a grand convergence of previously separated domains such as programmable-reconfigurable multi-processor architectures with embedded software, broadband radio, MEMS and biosensor interfaces.

When 30 nm MOSFETs will become available, chips will contain 2 billion logic transistors or the equivalent of 2000 programmable processors embedded in a reconfigurable network and 50 Mbyte of storage. The real bottleneck will not be in the process technology itself but in our ability to design products and services into such huge multiprocessor architectures on a single piece of silicon.

Deep-submicron Systems-on-Chip (SoC) are themselves distributed systems. They will be highly regular networks of programmable processors, compute accelerators, embedded memory and programmable mixed-signal acquisition systems that serve

post-PC application domains such as multimedia wearables, automotive systems, network servers and distributed ad-hoc sensor networks for ambient intelligence systems. The four major challenges for the design of these systems are: the control of power-density or energy consumption; co-design of heterogeneous, reconfigurable, multi-processor architectures together with their compilation environments; management of the data-transfer between the processing elements; mastering of signal integrity between analog and digital systems.

System design will be the translation of services into minimal energy distributed software running on processors that communicate using on-chip network protocols similar to the global network they are connected to. At the same time, energy distribution and power management over the chip will need tools and methods similar to the power management in the large systems.

Post-PC systems are global systems requiring co-design of the environment, sensors and SoCs. This requires the creation of teams of system and service designers, system-on-chip architects and IP creators. Traditional engineering schools are not prepared to create these “system and service engineers” of the future. This will require novel mixed university-industry system research organizations per-forming concurrent research and education on future integrated systems and services.

According to the author, there is an urgent need for worldwide efforts in system engineering research for the sub-100nm range. Otherwise we will not have the necessary engineering talent available to exploit the potential of the oncoming technology.

The third keynote presentation, entitled: “Electronic Nanotechnology and Reconfigurable Computing” was given by Seth C. Goldstein, from Carnegie Mellon University, USA. In this presentation, Chemically-Assembled Electronic Nanotechnology (CAEN) is investigated as an alternative to CMOS for constructing circuits with feature sizes in the tens of nanometers. In this approach, the properties of suitable molecules are exploited to conditionally connect cross-coupled sets of wires, thus generating a sort of a diode-resistor logic based on two-terminal molecular devices. The resulting structures, referred to as nanoblocks, are very regular, can be connected to CMOS circuits in order to interface the external world, and can be reconfigured, thus ensuring flexibility and defect tolerance. One circuit problem with this approach is the need of restoring the logic levels. This is achieved by a molecular latch which provides gain, fan-out and I/O isolation, and can be used as a memory element. The system architecture is hierarchical and comprises programmable nano-blocks interconnected to form clusters. The latter are in turn organized to form highly regular nanofabrics, deterministically built on top of CMOS. The main attributes of nanofabric are their hierarchical fabrication, their reconfigurability and their defect tolerance. This project involves research

issues spanning from Physics and Chemistry to Electrical Engineering, Material Science and Computer Science. More specific investigation areas comprise architecture, compilers, fault tolerance, circuit design and operating systems. Benefits are expected from the availability of billions of devices per square centimeter and by the ultra-low power consumption, as well as from the regular, homogeneous architectures and their fault tolerance. In contrast, the switching speed is not expected to exceed 10 MHz, well below its CMOS counterpart.

7. Enabling Technologies

The first invited presentation in this session entitled: “Optical networks – from dumb pipes to intelligent networks” was delivered by Marko Erman, from Alcatel, France. In this presentation the author depicted the evolution of optical networks, which enabled the development of Internet. The latter has brought the communication society into a new age: voice traffic has been gradually replaced by data communications; narrow band services are shifting to broadband, distance is no more a limiting parameter - within a click on the PC, the information crosses the ocean. By extension, this revolution was made possible thanks to the introduction of optical communication. The invention of single mode fibers, fiber-based optical amplifiers and semiconductor lasers together with wavelength multiplexing made it possible to transmit huge capacities over almost unlimited distances. As a result, a world-wide network, combining submarine and terrestrial networks, has been built. Optics has definitely won the battle of long-haul transport. But optical communication also dominates now the metropolitan networks, and starts to invade the access part, with the fiber to the home as the ultimate dream.

While initial benefits of optics were perceived largely on the transmission side, it is now also beginning to be considered as a serious candidate for routing. In fact, optics is gradually moving from “dumb pipes” to “intelligent networks”. The reason behind it is again linked to wavelength multiplexing, which basically consists in using a large number of wavelengths (up to 100 or even above) on the same fiber. Initially, it was seen as a good way to boost the fiber capacity, since it was easier and faster to add wavelengths than to increase the bit rate of the electronic circuits. But wavelength has also introduced a new granularity within the network. Rapidly, end-to-end wavelength services have emerged as an attractive proposition for operators. This led to the idea that routing - originally done within the network node by electronic means - can be done itself in optics, by simply switching the wavelengths. In a way, this concept introduces a higher degree of transparency within the network. The real motivation for this approach is, however, the cost. As the number of electro-optical conversions are reduced, the cost of the network elements is reduced as well. Transparency is not a concept easy to deal within a telecom-munication environment. Indeed, in order to guarantee a quality of service to the end user, a network needs to be monitored and managed. Transparency leads therefore to the interesting problem of how to monitor and supervise an optical channel, without interrupting the information flow. The talk reviewed these issues, illustrated them with recent research results, and discussed the remaining challenges and opportunities.

The second keynote presentation, entitled “Post CMOS devices” was given by George Bourianoff, from Intel Corporation, USA. The semiconductor industry has made progress during the last 40 years by scaling critical dimensions of CMOS

devices down in size, intro-ducing new materials and new device geometries. This presentation summarized that history, discussed current research into the ultimate scaling of silicon. According to the author, the limits of bulk CMOS will probably emerge after year 2015, potential limiters being: i) Lithography, ii) Diminishing performance returns from device scaling, iii) Interconnect scaling and, iv) Power dissipation. By year 2010 the clock speed is expected to increase up to 30 GHz, the transistor count will go up to 1.8 billion, but power density extrapolates up to 1000 W/cm^2, which is comparable to a rocket nozzle. Novel information processing devices, such as Single Flux Quantum devices, Quantum Cellular Automata, Tunneling Phase Logic Devices, Coherent Quantum Devices, Optical Devices and Molecular Devices were then reviewed by the author. These emerging technologies were parameterized in terms of their inherent speed, size, cost and energy requirements and compared to each other and to the human brain. The main conclusions of this presentation were that silicon-based CMOS is expected to be a major part of electronics for the foreseeable future; scaling along Moore's law will continue on planar bulk CMOS for at least 15 years, and performance scaling beyond CMOS will occur by integrating novel information processing devices on to silicon platforms. Thus, the new and emerging technologies will only expand the parameter space that can be addressed by silicon devices alone.

The third keynote presentation in this session was entitled: "Real world interactive computation and mobile computing", and was given by Jiro Tanaka, from Tsukuba University, Japan. Real-world interaction means extracting computer information using the real world objects as the key for information retrieval. It means connecting the computer to the "real world". By introducing real-world inter-active computation, we can realize the natural next-generation inter-face. Now, personal computers are common at home and everybody uses Internet. Personal Digital Assistants (PDAs) and mobile phones are very popular. In the near future, computers will be connected to the everyday objects and communicate among them by networks. Existing GUI and WIMP interfaces cannot be used because the displays of PDA or mobile phones are too small. Therefore, we need to develop post-GUI techniques which should be applicable both for small and large screen displays.

The "Real-World Interactive Computation" project aims to develop the elementary technology for real-world interactive computation and visual interface techniques for large screen displays. These techno-logies are also being applied to school education. This project involves 10 schools affiliated to the University of Tsukuba, with which cooperation has already started.

8. Emerging technologies

The first keynote presentation entitled: “Smart Dust” was given by Brett Warneke, from the University of California at Berkeley, USA.

The Smart Dust project aims to explore the limits of miniaturization by packing an autonomous sensing, computing, and communication system into a cubic millimeter mote that will form the basis of massive distributed sensor networks, thus demonstrating that a complete useful, yet complex, system can be integrated into ~1mm^3.

Because of the discreet size, substantial functionality, connectivity, and expected low cost, Smart Dust will enable entirely new methods of interacting with the environment, providing more information from more places in a less intrusive way than ever before.

Some examples of applications that we are targeting include defense networks that could be rapidly deployed by unmanned aerial vehicles (UAV) or artillery, racking the movements of birds, small animals, and even insects, virtual keyboards terrestrial and Martian weather-seismological monitoring, inventory control, product quality monitor-ing, smart office spaces, multi-hop communication networks, and interfaces for the disabled.

The second presentation in this session is entitled: “Prospect of superconducting digital electronics” was delivered by Akira Fujimaki, from Nagoya University, Japan, who presented the current status and future prospect of superconducting digital electronics. According to the author, superconducting integrated circuits based on the single-flux-quantum (SFQ) logic scheme have a high potential to overcome several limitations of semiconductor ICs, such as the increasing power consumption, the interconnect delay and the complexity crisis. An SFQ IC essentially consumes very low power because of the turn-to-zero (RTZ) nature of its signals, featuring a few picosecond duration. Furthermore, the RTZ means that the charging process of the interconnects is no longer needed. As a result, the throughput of the SFQ circuits can reach 100 Gb/sec. If high-end servers based on SFQ circuits are constructed in the future, higher performance resulting from the high throughput and from the broad band-width between processor and memory will be obtained. In addition, the power consumption problem will ease. High-throughput operation at 55 GHz has been demonstrated in a shift-register circuit. This circuit is constructed based on the advanced cell-based design technique; hence, it is easy to expand the circuit scale. Other potential applications such as a network switch for a high-end router, and an analog-to-digital converter for future base-stations were discussed. Potential problems of SFQ ICs are the development of suitable process and packaging technologies and the operation at very low criogenic temperatures, which makes the efficiency of the cooling system very

poor. Because of this, new materials other than Nb, allowing for somewhat higher temperatures (a few tens of K) are being explored.

The third presentation entitled: “Solid state implementations of quantum computers” was given by Göran Wendin, from Chalmers University of Technology, Sweden. In this talk an overview was given of the present research on several possible candidates for solid state implementation of quantum bits or qubits. The feasibility of quantum computing has been demonstrated with small molecular spin systems and atoms in cavities and traps. However, these systems are difficult to scale up to the large number of qubits necessary for useful computation.

The progress in microelectronics and nanotechnology makes solid state implementation of qubits promising candidates for quantum computers. Interesting solid state qubits include quantum mechanical two-level systems based on superconducting quantum dots and rings with Josephson junctions, semiconductor quantum dots with charge or spin degrees of freedom, atoms with nucelar spins implanted in solids, atoms stored above solid surfaces in microfabricated arrays of traps, and electrons trapped on helium surfaces.

A major problem with solid state qubits is the strong coupling to the environment, which may lead to fast decoherence and strong reduction in the number of useful operations. This problem may be tackled by using superconducting devices with built-in macroscopic phase coherence, by using qubit systems which interact relatively weakly with the environment, like spin systems, or by designing systems where the coupling to the qubits can be controlled, via “tuneable” links or physical displacement of the qubit, e.g. atoms in micro-electro-mechanical traps.

9. Wrap-up session

The main conclusions drawn from the wrap-up session may be summarized as follows:

- The R&D efforts will continue despite the economy downturn;
- Ubiquitous computing is going to fill-up and dwarf the currently overgrown bandwidth capacity and to exploit its flexibility and seamless-ness for office, travel, car, home and environment applications;
- A key point will be its ease of use (human interface), and the efficiency of the infrastructure (broadband, routing, access, etc.);
- Post-PC systems are global systems requiring co-design of sen- sors, RF circuits and SoCs, thus requiring a grand convergence of previously-separated domains of expertise;
- Optical networks will dominate the communication infrastructure;
- Wavelength multiplexing and all-optical routing will expand in the future, thus intelligent networks will replace pure communication pipes;
- New physical principles and new device concepts are needed to develop flexible routing via all-optical switching;
- CMOS technology will dominate the digital world for the next 10-15 years;
- Emerging technologies are unlikely to fully replace CMOS in the foreseeable future; rather, they can complement CMOS by simply extending some of its capabilities;
- Micro- and nanoelectronics will have a strong impact on Biology evolution by allowing critical control of gene states at the single-cell level; this will require inter-disciplinary efforts in order to tackle problems of unprecedented complexity;

In the following, the main issues, strengths and weaknessess regarding each of the suggested enabling and emerging technologies are briefly reported:

CMOS

- Handling design complexity, new architectures, new functions;
- Interconnect delay, on-chip optical communication;
- Power dissipation, heat extraction and power management;
- Alternative low-cost lithographic tools (imprint, self-assembly) as opposed to EUV, X-rays, ion beam.

Optical integrated components and networks

- New components for all-optical networks (non-linear crystals, optical switching, multiple wavelength devices, etc.);

- Issues: integration of arrays;
- Power consumption;
- Critical breakthrough needed for materials (integration on Si).

Molecular/Bio Electronics

- Issues: system architecture, fabrication, thermal stability, circuit design;
- Strength: potential low-cost fabrication by self assembly.

Interaction of microelectronics and biology

- Issues: terminology, reliability, manufacturability, design, safety.

Superconducting SFQ integrated circuits

- Issues: cooling, power, integration scale;
- Compared with cooled CMOS, how does it stack up?
- New materials, such as NbN allowing for 12 K operation;
- Difficulties in HTC – integration, pure quality;
- New applications: ADC?

Quantum information systems

- Issues: scaling, output, architectures, programming, decoherence;
- Killer application: secure communication, cryptography.

Smart Dust

- Issues: energy efficient communication systems, efficient power sources, location, social and environmental problems;
- Convergence of intelligent systems;
- Vast number of applications.

In a competitive world, the above trends will be efficiently pursued by taking care of a number of human factors which appear to play an essential role in promoting such technology developments:

- Civilization
- Creativity
- Visionary government policy
- Enterprises

- Proactive technology community
- Organization
- Education

10. Reflections by Ralph K. Cavin III

I have the privilege of serving on the International Organizing Committee for the IWFIPT; a workshop designed to project long term trends in information technologies across a wide spectrum of areas. Typically, the workshop examines underlying technology trends as well as emerging and evolving areas of application for the technologies. The workshop has a unique format in that each of the sponsoring regions (Asia, Europe, and North America) provides a speaker on a topic at each of the sessions. Due to the wide scope of workshop topics, the IWFIPT is not a meeting of specialists in one technology area, but rather a meeting attended by a few specialists from each of a broad range of technologies. Attendees benefit from the insights gained by exchanging ideas with colleagues who work in complementary disciplines. The 4th IWFIPT was held in Gubbio, Italy, from September 3-6, 2001, and was hosted by the European Com-mission, ERCIM, and the University of Bologna. The general chair was Professor Giorgio Baccarani of the University of Bologna. For those interested in the details of the meeting, including the agenda, the presentation materials, and a meeting summary, these materials are available on the web site www.iwfipt.unibo.it.

One of the impressions from the workshop is that the pace of technology evolution is continuing unabated. In almost every area, from semiconductors to optical networks, there are significant technical challenges, but there is quite a bit of confidence that they will be overcome to enable continued advance in capabilities. Revolutionary technologies that are being proposed seem to offer much promise, but face extraordinary implementation challenges that may make it difficult for them to supplant rapidly advancing technologies in their existing application domains. On the other hand, it seems that these radical technologies may find their way into the mainstream by addressing niches that cannot be well addressed by existing technologies. One example from the workshop was the use of nanotechnology to form nanometer-scale channels for use in DNA analysis. On that topic, there are enormous opportunities for the use of nanotechnology to enable a deeper understanding of the processes that underlie the operation of the living cell. As impressive as the accomplishments of the human genome project were, we seem to have decoded the “ROM” of living systems but don’t know very much about its “Operating System”.

There was quite a bit of emphasis on various forms of communication technologies at the workshop ranging from ubiquitous RF networks to digital home networks to optical networks. I think that we will see a continued proliferation of localized and wireless networks for home, business, and local areas that are ultimately connected to large backbone wide area networks. To a non-specialist, the standard format of overview presentations on this topic begin with a picture depicting interconnections

of the various types of networks with an alphabet soup of labels describing the various communications protocols and technologies. This is similar to the propensity of those of us in semi-conductor technology to draw logarithmic plots depicting technology evolution! When we eventually get low cost, high bandwidth service to the home, it appears to me that the utilization of the network infrastructure will grow rapidly. This would be a welcome development because today fiber networks do not appear to be fully utilized. There seems to be a sort of quantized growth phenomenon associated with the addition of new bandwidth in optical networks, not unlike the growth of DRAM memory sizes. Apparently, the addition of a new increment of capacity is not immediately followed by a corresponding increase in utilization of that capacity. To some extent, further increases in network capacity must await growth of utilization of existing capacity, often driving user price discounts.

It is truly amazing the extent to which electronics has pervaded automotive applications. Visions of the future show continued growth in electronics utilization, perhaps ultimately taking the driver out of the loop in some situations. In another application area, the PDA of the future may not only provide for many of the transactions of our lives, but also may become a kind of personal diary of our lives. For example “memory prosthesis” proposes to capture and store, in a searchable format, events in our lives such as meetings with professional colleagues. It seems to me that we are quite a way from making this sort of thing a reality because it would require enormous memory and very sophisticated processing that we don’t know how to implement with today’s technologies. (To say nothing of the social implications of such advances!)

We always review the status of CMOS technology at the IWFIPT and each time, we conclude that CMOS technology has a lot of life left. When we survey the horizon for new replacement technologies, we see many possibilities but, upon closer examination, they all seem complementary in some way to CMOS and not so much a competitor. As CMOS approaches 10 nm features, it is beginning to approach the scales of some of the proposed molecular alternatives. Moreover, large scale assembly technologies for proposed molecular alternatives do not now exist. One interesting idea that was articulated was that logic in the future might be implemented via interconnection of regular arrays of extraordinarily dense elements, thereby circum-venting the need to interconnect irregular structures and facilitating the development of self-assembly methods for fabrication.

A recurring theme in the workshop is the increasing importance of growing energy consumption by integrated circuits. It appears that design can buy us significant reductions in energy consumption though multiple VT and multiple VDD circuits, through scheduling of power usage and through architectural innovation. One difficulty with the voltage scaling strategy is that noise margins may be decreased

due to the loss of headroom between VDD and VT. Nevertheless, the ability of design to forestall the effects of increased energy consumption is ultimately limited and advances on the technology side are also needed. In distributed and autonomous systems, energy scavenging, dense energy storage technologies, and very low power utilization are usually very important. In high performance applications, the level of energy consumption per unit area of silicon is near that of a hot plate, and thermal heat removal problems are paramount.
The salient trends that were identified in the concluding session of the 4th IWFIPT are:

- Total system view is predominating the isolated device view
- The importance of design and design disciplines in achieving the Moore's Law cadence
- The increasing heterogeneity of systems
- Persistence of CMOS technology evolution
- Human resource needs
- Power and energy
- Importance of interfaces.

Appendix 1: Committees

International Steering Committee:

Shojiro Asai, *Hitachi*, Japan
Giorgio Baccarani, *Università di Bologna*, Italy
Ralph Cavin, Semiconductor Research Corporation, USA

European Committee:

Giorgio Baccarani, *Università di Bologna*, Italy
Daniel Bois, *GemPlus*, France
Kostas Glinos, *European Commission*, Belgium
Peter Knight, *Imperial College*, United Kingdom
Pierpaolo Malinverni, *European Commission*, Belgium
Marc Van Rossum, *IMEC*, Belgium

Asian Committee:

Shojiro Asai, *Hitachi*, Japan
Yasuhiko Arakawa, *University of Tokyo*, Japan
Hisatsume Watanabe, *NEC*, Japan
Toshiaki Ikoma, *TI Japan*, Japan
Toshiro Hiramoto, *University of Tokyo*, Japan
Tetsuhiko Ikegami, *Aizu University*, Japan
Tetsuo Nakamura, *Fujitsu*, Japan
Nobuyuki Toyoda, *Toshiba*, Japan
Toyoki Takemoto, *STARC*, Japan
Yoichi Unno, *SIRIJ*, Japan

North American Committee:

Ralph Cavin, Semiconductor Research Corporation, USA
Dan Radack, DARPA, USA
Steve Hillenius, Lucent Tecnhologies, USA
Kang Wang, University of California Los Angeles, USA
Rajinder Khosla, National Science Foundation, USA
Tom Jackman, NRC of Canada, Canada
Bob Doering, Texas Instruments, USA
Gernot Pomrenke, US Air Force Office of Scientific Research, USA
George Bourianoff, Intel Corporation, USA

Appendix 2: Conference Programme

Monday September 3, 2001

I. FUTURE SYSTEM AND TECHNOLOGY CHALLENGES - 1

A. The ultimate personal companion: challenges for technology development
Heikki Huomo, Nokia

B. Ubiquitous networking
Jan Kruys, Agere

C. Digital home networks
Ryoichi Sugimura, Panasonic OWL

II. FUTURE SYSTEM AND TECHNOLOGY CHALLENGES - 2

A. Optical Network Internet Infrastructure
Toshitaka Tsuda, Fujitsu

B. Convergence between IT and automotive: technology challenges for the 2020 car - Europe

C. At the interface between information technology and biology
Harold Craighead Cornell University

Tuesday September 4, 2001

III. SILICON EVOLUTION

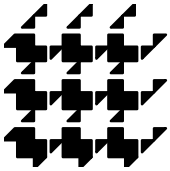
A. Low Power CMOS
Tadahiro Kuroda, Keio University

B. System-on-Chip Design Challenges in the Post-PC era
Hugo De Man, IMEC

C. Reconfigurable computing
Seth Goldstein, Carnegie Mellon University

IV. POSTER SESSION

FET - Future and Emerging Technologies



DIMACS — Center for Discrete Mathematics & Theoretical Computer Science

This workshop is part of a series of strategic workshops to identify key research challenges and opportunities in Information Technology. These workshops are organised by ERCIM, the European Research Consortium for Informatics and Mathematics, and DIMACS the Center for Discrete Mathematics & Theoretical Computer Science. This initiative is supported jointly by the European Commission's Information Society Technologies Programme, Future and Emerging Technologies Activity, and the US National Science Foundation, Directorate for Computer and Information Science and Engineering.

More information about this initiative, other workshops, as well as an electronic version of this report are available on the ERCIM website at http://www.ercim.org/EU-NSF/

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